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A NEW CMOS FIRST GENERATION CURRENT CONVEYOR CCI

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Abstract: *This paper presents a new and improved first generation current conveyor (CCI). The proposed circuit is based on a CMOS translinear loop and self-cascode current mirrors. The principle of the circuit is analysed. PSpice simulation results for the proposed cicuit in 0.3μm CMOS technology are given to verify the theoretical analysis.*
Key words: *current conveyor, self-cascode mirror, CMOS*

1. INTRODUCTION

Since 1968 when Sedra first published CCI, current conveyor based circuits have received lots of attention in analog signal processing applications, such as filter (Yamacli et al., 2008)function generator(Minhaj, 2009), impedance function synthesis (Yuce, 2008), etc. (Di Carlo et al., 2009).CCs are unity-gain amplifiers widely used by analog designers, in particular because they offer a number of advantages,such as better linearity, wider bandwidth, and design flexibility over conventional voltage-mode active devices.

Several types of CC exist covering first, second (CCII) and third generation (CCIII). Whilst CCII is considered the most versatile and used CC, the first generation CCI is well known for its simplicity.

The definition matrix (1) along with the impedance levels (Tab.1) presents the main characteristics of the ideal CCI (CCI+ and CCI-). The CCI symbol and CMOS structure are given in Fig. 1 and Fig. 2. A good CCI structure must provide several features: very low X input impedance, very high Y and Z impedance, unity voltage and current gains between ports, large dynamic input and output current and voltage ranges. The typical CMOS structure (Fig.1) is a class AB current is a class AB current conveyor that offers the advantages of high dynamic range, wide bandwidth and non-slew rate limited performance. Due to the low quality of the simple current mirror (CM) this CCI structure assures moderate performances in respect of input/output impedance.

Several papers present AB class current conveyors using improved current mirrors: cascode mirror (Minaei, 2003), high-swing mirror (Calvo et al., 2003), low voltage self-cascode (Kaur et al., 2008), etc.

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

Node (CCI)	Impedance Level
X	0
Y	∞
Z	∞

Tab.1. CCI impedance levels

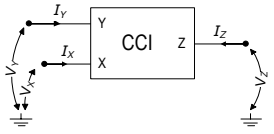

Fig. 1. CCI symbol

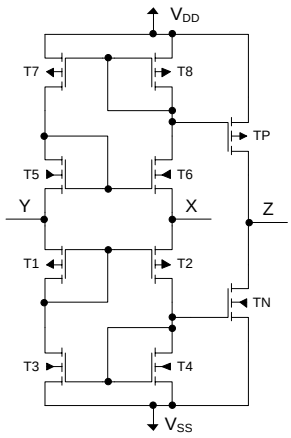

Fig. 2. Typical CMOS CCI+ structure

The purpose of this paper is to propose and analyse a new AB class CCI structure based on self-cascode mirrors (SCCM). This structure improves input/output impedances without affecting voltage dynamic ranges.

2. NEW SELF-CASCODE CCI

The proposed circuit is given in Fig.3 and based on 6 SCCMs (Fujimori, 1999). A well-designed SCCM assures output resistance similar to that of the cascode mirror but output voltage similar to the simple CM (Dragoi, 2010).

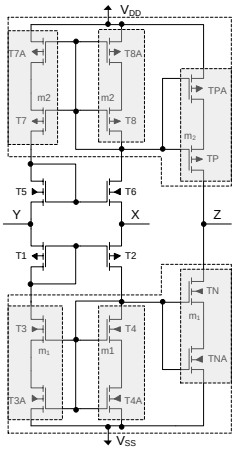

Fig. 3. New self-cascode CCI+

CCI+ new	*W*[μm]	*L*[μm]
T_1, T_2	26	3.3
T_3, T_4, T_N	68.4	1
T_{3A}, T_{4A}, T_{NA}	3.8	0.65
T_5, T_6	10.2	2.8
T_7, T_8, T_P	96	0.55
T_{7A}, T_{8A}, T_{PA}	32	3.4

Tab.2. W and L sizes for self-cascode CCI+

Input and output resistances:

$$R_X \cong \left(\frac{g_{ds2}g_{m4}+g_{ds4}g_{ds4A}}{g_{m2}g_{m4}g_{m4A}} + \frac{g_{ds1}g_{m3}+g_{ds3}g_{ds3A}}{g_{m1}g_{m2}g_{m3}}\right) || \\ || \left(\frac{g_{ds5}g_{m7}+g_{ds7}g_{ds7A}}{g_{m5}g_{m6}g_{m7}} + \frac{g_{ds6}g_{m8}+g_{ds8}g_{ds8A}}{g_{m6}g_{m8}g_{m8A}}\right) \quad (2)$$

$$R_Y \cong \frac{g_{m3}}{g_{ds3}g_{ds3A}} || \frac{g_{m7}}{g_{ds7}g_{ds7A}} \quad (3)$$

$$R_Z \cong g_{mN}r_{oN}r_{oNA} || g_{mP}r_{oP}r_{oPA} \quad (4)$$

All the transistors must be designed to work in saturation and for a standard 0.35μmCMOS technology the pMOS transistors must be sized using short channel effect (SCE) (Zeki&Kuntman, 2000) and nMOS transistors using reverse short channel effect (RSCE) (Dragoi, 2010).Tab. 2 shows W and L sizes for all transistors.

3. SIMULATION RESULTS

The circuit was designed and simulated in 0.35μm CMOS technology using a PSpice simulator. Power supplies of±2.5V and of the sizes in Tab. 2 give a self-bias current of 55μA. This table shows the input and output impedances, voltage and current gains, bias currents and active areas for the proposed CCI+ and for a typical CCI+.For almost the same active area the new CCI provides the same input resistance on port X but the bias current is halved.There are good improvements in respect of input impedance on port Y –13.5 times and output impedance on port Z – 8 times. Current gains β and γ errors are reduced from 0.7% to 0.11%. Voltage gain α is reduced from 0.72% to 0.38%.

Fig.4 shows input and output impedance for both the new CCI+ and a typical CCI+.

	CCI+ new	*CCI+ Typical*	
Technology	CMOS 0.35μm, ±2.5V		
Active area	926	881	μm^2
Bias current	55	110	μA
Rx	20.02	19.12	Ω
Ry	6.86	0.507	MΩ
Rz	10.89	1.36	MΩ
V_X/V_Y *(α)*	0.9962	0.9928	
I_Z/I_X *(β)*	1.0011	1.007	
I_Y/I_X *(γ)*	0.9989	0.993	
Cy	105	130	fF
Cz	85	55	fF

Tab. 3. New CCI+ versus typical CCI+ performances

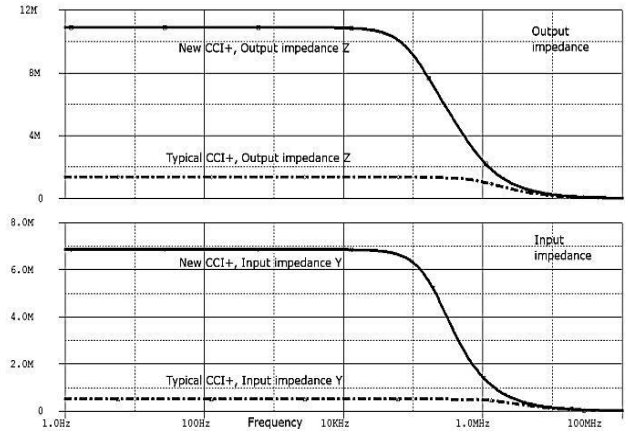

Fig. 4. Input/output impedances for new and typicalCCI+

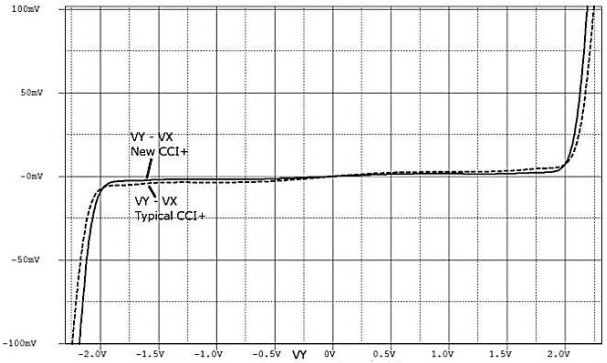

Fig. 5. Input voltage tracking error between ports Y and X

Fig. 5 presents the voltage tracking error between Y and X. It can be seen that the input voltage range is almost the same for the new CCI as for the typical CCI based on CM.

4. CONCLUSION

This paper has presented a novel CCI structure based on self-cascode current mirror. The results show that the proposed circuit improves performances in respect of input/output impedances and voltage/current gains maintaining large dynamic voltage ranges.

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