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CHARACTERIZATION OF A 40 KHZ PHASE-LOCKED LOOP USING AGILENT SPECTRUM ANALYZER

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***Abstract**: A prototype 40 KHz Phase-Locked Loop (PLL) has been designed and fabricated in Instrumentation and Informatics Research Laboratory, Department of Electronics and Communication Technology, Gauhati University, Assam, INDIA. The system has been tested using Agilent Spectrum Analyzer (Model: N9320; Frequency range: 9 KHz–3 GHz),* Tektronix 100MHz arbitrary function generator (Model: AFG3012, 1GS/s) and *Digital Phosphor Oscilloscope (DPO) (Model: Tektronix TDS 3052, 500MHz, 2.5 GS/Sec). This paper presents in details the experimental results and characterization of phase noise of the prototype PLL.*
***Key words**: PLL, Spectrum Analyzer, DPO, phase noise*

1. INTRODUCTION

The PLL is an electronic control system that synchronized the output phase and frequency of a controllable oscillator to match the phase and frequency of a reference signal. Ideal steady state condition shows zero difference in phase and frequency between the controlled oscillator output and the reference signal frequency (Stanley Goldman, 2007). PLL was first described by Appleton in 1923 and de Bellescize in 1932 (Nikolaos I. Margaris, 2004). It has contributed significantly toward the technology advancement in modern communication system. The theoretical description of PLL was well established in the late 1970's, but widely used in modern communication systems after rapid development of integrated circuits (IC) during the period (Guna-Chyun Hsieh and C. Hung, 1996). The PLL improves the performance and reliability of modern electronic systems, especially in common electronic appliances used in daily life.

PLLs are used to implement frequency synthesis, clock and data recovery, high frequency clock generation and as a local oscillatior for RF system (W. Rhee and A. Ali, 1999). Any jitter or phase noise in the output of a PLL used in these applications abruptly degrades the performance of the system (Salvatore Levantino, Stefano Pellerano, 2004). As such the study of jitter or phase noise of PLL is of great importance for any communication systems. The noise performance of any PLL must be evaluated in presence of large signal behavior.

So, we have designed, fabricated and tested a prototype PLL for characterization and study of noise performance using Agilent Spectrum Analyzer for low frequency application (e.g. radio receiver) in communication system.

2. THE BASIC BLOCK OF PLL

The PLL consists of four basic functional blocks – voltage controlled oscillator (VCO), phase frequency detector (PFD), loop filter (LF), and frequency divider (FD) (Stanley Goldman, 2007). The PFD output signal is a function of the difference between the phases and frequency of reference frequency and FD frequency (Jack Smith, 2003). The PFD output is filtered, amplified and then applied to the VCO. The PFD output forces to change the frequency of VCO in a direction that reduces the difference between the input frequency and the FD output frequency. If the two frequencies are significantly close, the feedback mechanism forces the two PD frequencies to be equal and the VCO is locked with the incoming phase and frequency. When both signals are synchronized, the PLL is said to be in lock condition. The phase error and frequency difference between the two signals is always zero under this condition. (William F. Egan, 1998)

3. THE PROTOTYPE PLL

The prototype PLL hardware that we developed in our laboratory is shown in Fig. 1 below. The system is designed and fabricated using conventional electronic components easily available in the market. A separate power supply unit is developed for driving the PLL hardware which is shown in Fig. 2.

Fig. 1. The PLL Hardware

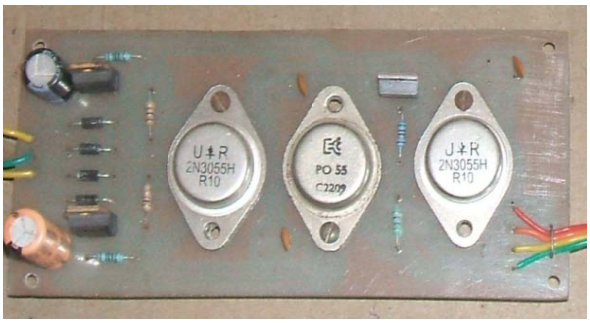

Fig. 2. Power Supply unit

4. THE EXPERIMENT

The experimentation on the prototype PLL is performed using Agilent Spectrum Analyzer (Model: N9320B, Frequency range: 9 KHz – 3 GHz), Tektronix 100MHz arbitrary function generator (Model: AFG3012, 1GS/s) and Tektronix 500 MHz Digital Phosphor Oscilloscope (DPO) (Model: Tektronix TDS 3052, 2.5 GS/Sec). Fig. 3 shows the measured output in the

time domain when the circuit is locked to 40 KHz reference (10.0 MS/s, 10K points). Fig. 4 shows the extended wave form of fig. 3 to explain the peak to peak noise jitter profile of the output (500 MS/s, 10K points).

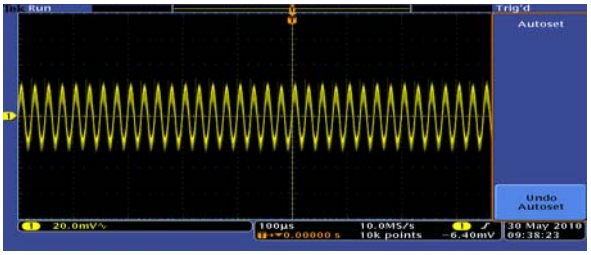

Fig. 3. Measured output of PLL in time domain

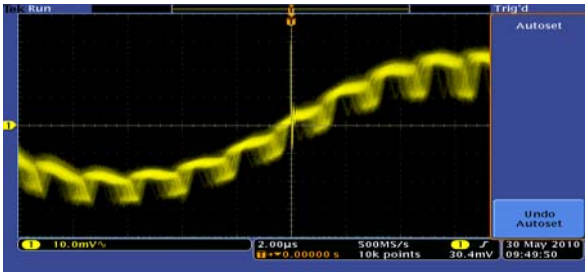

Fig.4. Extended output of PLL

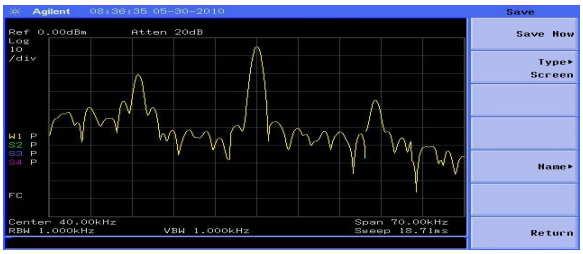

Fig.5. Spectrum of output signal

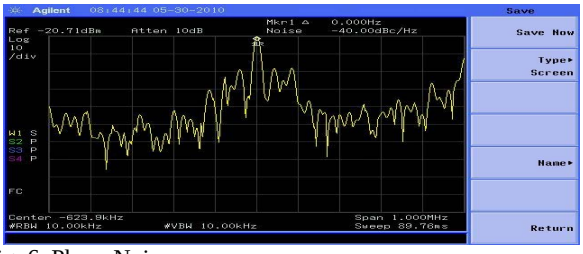

Fig. 6. Phase Noise

Fig.7. Occupied bandwidth

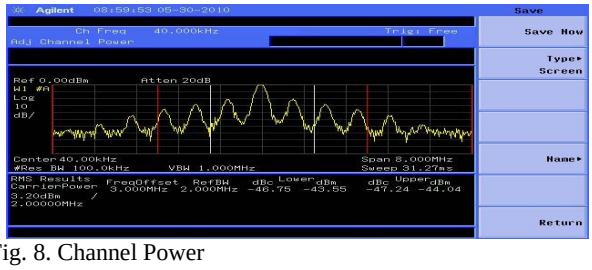

Fig. 8. Channel Power

Fig. 5 shows the spectrum of the output signal close to the carrier. The spectrum contains spurious components. The video bandwidth (VBW) is recorded as 1 KHz. Fig. 6 shows the phase noise profile to the same output. It is observed that the phase noise of the system is – 40dBc/Hz.

Fig. 7 shows the occupied bandwidth (OBW). It is seen that the OBW is 85.04 KHz. The % power of OBW of the system is recorded as -26.00dB. From fig. 8 it is seen that the lower channel BW power is – 46.75dBc (– 43.55dBm) and upper channel BW power is – 47.24dBc (– 44.04dBm). The total carrier power of the system is 3.2dBm/2MHz.

5. DISCUSSION AND CONCLUSION:

The overall phase noise of PLL synthesizer depends on LF bandwidth, phase noise of the PD and free running VCO phase noise (Petr Vagner, Petr Kutin, 2006). The RF spectrum analyzer is use to measure spectral density directly, provided that the phase noise of the source under test is significantly AM noise. Limitations of this method are phase noise of the spectrum analyzer local oscillator, dynamic range and resolution.

The paper presents the characterization of the prototype PLL system that we have developed in our laboratory. The output frequency of the PLL synthesizer is 40 KHz with a phase noise of – 40dBc/Hz. The output spectrum is with jitter and there are some spurious signals close to the first harmonic. To realized the PLL synthesizer requires fine tuning in its design and can be used in low frequency communication systems with low phase noise. In future work we propose to evaluate the other noises present in the present system.

6. ACKNOWLEDGEMENT:

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