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A FAST CAMERA WITH ONLINE IMAGE EVALUATION

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Abstract: *The paper describes an implementation of a smart high-speed camera system based on FPGA structure. The main goal is an automatic detection and calculation of the laser beam position on a projection screen. Maximum required processing data rate is five hundred frames per second with the image resolution 1280 x 1024 pixels.*
Key words*: FPGA, DSP, LVDS, image processing*

1. INTRODUCTION

Modern control systems require in some cases special approach to data acquisition and data processing. Computer vision is undoubtedly one of these cases. Currently both, sensing methods (camera chips, optics, data transfer and storage) and processing algorithms are well prepared for usage. General problem of these methods is a necessity to process huge data amount as fast as possible.

Traditional approaches use PC AT platforms for data processing very often. Advantage of this solution is in availability of components and high level of flexibility. On the other hand, this concept suffers from several disadvantages, which make practical use in real-time applications processing huge amount of image data with strict limits on power consumption and system physical dimensions impossible.

One of the applications that require non-traditional solution is fast camera with real-time tracking of laser beam mark on the projection screen in shooting-range simulator.

2. TECHNICAL REQUIREMENTS ANALYSIS

A Shooting – range simulator consists of projection screen where simulated battlefield with targets is shown. Standard data projector is used to create images on the projection screen.

Shooters in the simulator use guns equipped with infrared laser LED that creates spots on the projection screen. This spots mark exactly the places the shooters are aiming at. Main objective of the project was to design and implement camera system that would be able to detect spots from up to ten guns. Required position sampling frequency was 50 Hz for each gun. Precision of beam position measurement should be better than one millimeter. Projection screen dimensions were defined as 1.2 m x 1 m.

Time division multiplexing is used to distinguish between guns. It means that each gun's laser beam shines only one tenth of sampling period. Required fifty samples per second and per each gun give us necessity to process 500 frames per second.

Required detection precision (1 mm) defines maximal size of the camera pixel. Considering whole projection screen (1.2 m x 1.0 m) we need to use sensing element with at least 1200 x 1000 pixels.

Specification proposed in previous paragraphs determines required chip parameters.

The nearest higher standard resolution of camera chips is 1280 x 1024 pixels. Required frame rate is 500 frames per second. Dynamic range necessary for detection was specified as 60 dB (at least 10 bits per pixel). Because of short exposition time and signal to noise ratio, size of sensing element on the chip was important and ability of reading data of one picture

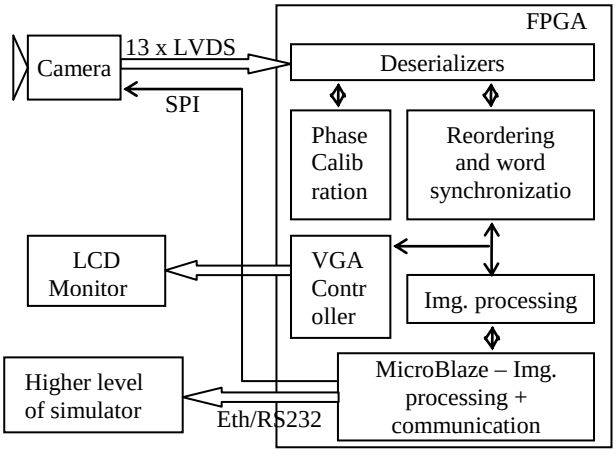

Fig. 1. System architecture overview

while the next one was being taken was required (latent image). The last important chip characteristic was sensitivity in the part of spectrum, where IR lasers radiate. Digital camera chip CMOS *CYIL2SM1300AA* from Cypress semiconductors (Cypress 09) was finally selected. It fulfilled all the requirements.

Simple calculation gives us a result that it is necessary to process approximately 780 MB per second in nonaligned 10-bit data format. It means processing of one pixel can take at the most 1.5 ns.

Even only transfer of such a data volume requires special optical interfaces or e.g. 10 Gb Ethernet that is also not yet easily available solution. System based on x86 family processors could cope with it in multiprocessor configuration, but it would meet neither power consumption requirements (max 8 W) nor spatial limits (15 x 15 x 30 cm). Signal processor (DSP) based solution would require design of glue circuitry between CMOS chip and DSP data busses, design and manufacturing of complicated PCBs, what would make device too expensive.

FPGA based architecture was chosen as a solution.

3. SOLUTION

Block scheme of the proposed solution can be found on the figure 1. The camera chip is connected directly to the FPGA. Data flow 780 MB/s generated by the camera chip is divided into twelve high-speed data channels. The thirteenth channel is used for control information transfer (start/end of frame, test patterns, checksums etc.). As a physical layer, differential LVDS interfaces working in double data rate mode is used for each channel. Working frequency can be set from 40 to 320 MHz (80 to 640 Mbit/s) depending on required frame rate.

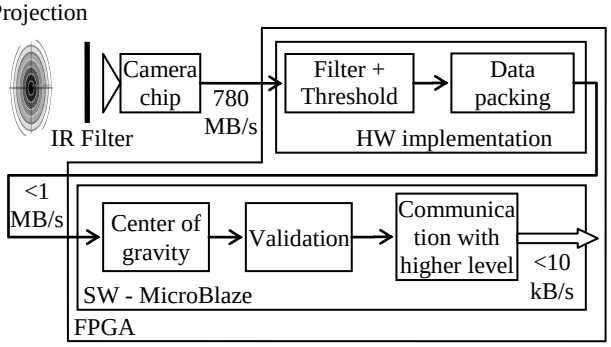

Fig. 2. Image processing block scheme

Additional SPI connection from the soft core processor MicroBlaze to the camera chip is used for control purposes – resolution, frame rate setting etc..

Even though high performance families Virtex 4 and Virtex 5 would offer more comfortable implementation, in order to keep camera price as low as possible, cheaper device family Xilinx Spartan-3E was chosen (Xilinx 09). Implementation of the described interfacing circuitry for so high frequencies is on the upper bound of this device performance and becomes serious issue to solve. The input pin placement and deserializers logic had to be planned and optimized manually to fulfill all timing requirements.

The next issue implied by high-speed interface usage is unknown phase relation between clock signal and data lines. Automatic phase calibration had to be implemented. Camera chip is configured to transmit well-known test pattern (01010101) on the system start. The calibration state-machine changes phase shift to find both signal edges and evaluates optimal phase position.

After calibration unit finds the best phase shift for data sampling, synchronization on the word level has to be established. Up to now, we worked on the bit level, now we need to find the beginning of words in the stream of bits to be able to decode them. This is done using different test pattern transmitted by camera chip. Synchronization state machine finds the pattern in the stream and locks on it. From now on, we can decode the data.

As mentioned before every pixel value is represented by 10-bit word in the camera. Stream of 10-bit words is mapped on twelve serial data lines of interface. To do this, chip uses sophisticated algorithm defined by the vendor. Next operations that FPGA has to apply on data are deserialization and reordering. After that, we get stream of pixel data. At maximal rate, we get 655 million of 10-bit data words per second. Reordered data stream represents image and can be finally used for image processing.

The chain of image processing steps is shown on figure 2. The first step of image processing block is separation of laser beam spot from background. Data projectors used in simulator produce practically no infrared light. Because level of infrared light from other sources in the shooting – range room is also very low, we can use optical filter that lets pass infrared part of spectrum only to separate laser beam from background. After this filtration, we get contrast image where laser beam is bright spot on much darker and nearly constant background. These conditions enable us to use simple threshold technique – described in e.g. (Sonka 2007) – to identify pixels belonging to laser beam spot.

The next task is to find the position of the spot. In order to achieve highest possible system flexibility the searching task is divided between hardware and software. Software is run in soft-core processor MicroBlaze that is implemented in the FPGA fabric. The hardware processes raw data stream, performs thresholding and sends to processor information about pixels that pass the threshold. Pixel values are packed together with their coordinates in data packing block and passed on to the processor. Considering that laser spot should not fall into more than four pixels, data amount is largely reduced in comparison with raw data. Data throughput is maximally in orders of hundreds of kilobytes per second.

$$x_T = \sum_i \frac{m_i x_i}{m},\ y_T = \sum_i \frac{m_i y_i}{m},\ m = \sum_i m_i \quad (1)$$

These data are further processed in the software. Equations (1) are used to calculate center of gravity of found spots – where x_i and y_i are pixel coordinates, m_i is pixel value. Center of gravity gives us very good estimate of real center of laser beam spot even though picture is not ideally focused or there is some noise in the image (Hauβecker, 1999). Validation block further reduces number of false spots based on distance from spot in previous frames. Validated coordinates are passed to the higher level of shooting – range control system that was not part of the project.

The processor can be connected to the higher level of the control system through either 100 Mbit Ethernet interface or serial port, which speed is acceptable because only spots coordinates are transferred (data flow in orders of kB/s).

For easier camera installation, mainly position and focus adjusting, a VGA output was added. This output shows what exactly camera can see.

Basic parameters of the system are summarized in the table 1.

Parameter	Value	Units
Clock frequency	40 – 320	MHz
Bitrate per channel	80 – 640	Mbit/s
Number of processed data words	96 – 768	Mwords/s
Frame rate (10 guns)	50 – 500	Hz
Samples per gun	5 – 50	1/s
Max. power consumption	6	W
FPGA Spartan-3E1200 utilization	63	%
- Camera core	21	%
- MicroBlaze system	42	%

Tab. 1. Parameters summary

4. CONCLUSION

The project resulted in fully functional prototype which met all requirements. The solution was verified in real application. The proposed camera system is currently commercially produced and commonly used in shooting range-simulators.

Future work will be focused on multiple camera synchronization in order to increase screen dimensions.

5. ACKNOWLEDGEMENT

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